DESIGN AND IMPLEMENTATION OF LOW POWER THERMAL AWARE ATM

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ABSTRACT

In this Paper, we have designed a Automated Teller Machine (ATM) which is electromechanical machine works in different temperature. We analysed the Static Power at discrete temperature that is thermal scaling of ATM at XILNIX 14.1 ISE Design Suit. In this paper we have used two FGPA family one is Spartan which is Spartan 6 and another is Virtex which is Virtex 4. We have distinguished on chip power by varying the Ambient temperature from 50°C to 5°C and we observed when we lowered the temperature of both FGPA families automatically the leakage power lowered that determine our ATM are worked in any temperature without disturbing its functionality.

KEYWORDS- *Ambient Temperature, Thermal Scaling, Xilinx, Verilog, FGPA.*

I. INTRODUCTION

The environment is where we all meet's where all have a mutual interest it is one thing we share. Environment plays a vital role in our life. Day by Day people totally depend on science and technology but somewhere it harms our environment so we implement harmless and hazardous designs that Conserve energy. One of the best innovative technology used in 21st century is Automatic Teller Machine (ATM) .It is an electronic banking outlet that allows customer to complete basic transaction without the aid of a branch representative or teller. ATM machines are super intelligent machine it operates at each and every temperature. Increasing levels of integration in Field Programmable Gate Arrays, have resulted in high on-chip power densities, and temperatures. The heterogeneity of components and scaled feature sizes in Platform FPGAs have made them vulnerable to various temperature dependent failure mechanisms. Junction temperature is directly related to power dissipation, thermal resistance and Ambient temperature and the function of the heat sink is to provide lowest possible thermal Resistance between the junction and its environment- assuming environment is always cooler. As our ATM will consume low power, there will be less use of electricity and thus less use of natural resources of the planet. Low Power design is a necessity today in all integrated circuit that's why we design ATM which is low power design. Today scientist and researchers are focusing toward power consumption. These are efforts to Reduce Dynamic and well as static Power consumption. The benefits of low power are clear. At the system level, low power allows FPGAs to be utilized in power-sensitive designs—particularly important for systems with very low quiescent power. The RTL schematic of the ATM is shown in Figure.1.
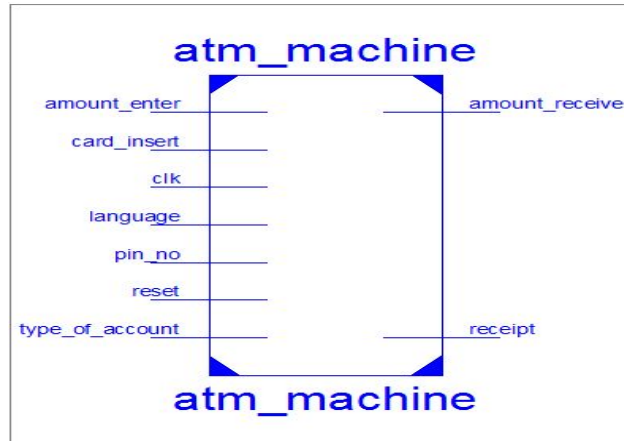
Figure. 1 RTL Systematic of the ATM

II. EXPERIMENTAL SETUP

We implement our work on XILNIX ISE design suit and the code of the ATM is written in Verilog hardware language. It is much used in design and verification of digital circuit at the Register transfer level of up to both the FGPA that is 0.1ns or 10GHZ with a duty cycle 50%.

III. RELATED WORK

B. Pandey et.al proposed which FGPA family is more power efficient. It comparing Spartan 6 FGPA with Virtex 4 FGPA at Different temperature. It estimates the Linkage Power by Varying Discrete Ambient Temperature .and specify which is better [1]. M.Chmeil* et.al proposed the one-bit word dual central processing unit, the purpose of this design is comparing the obtained performance with the general-purpose Microprocessor [2]. B. Pandey and Ravikant Kumar have proposed the effect of using digitally controlled impedance I/O standard in memory interface design in terms of Power consumption and also LVDCI-23 is the highest power consumer and the LVDCI-12 is the lowest one [3] Tim Tuan et.al proposed a design and implement of Pika a 90nm low FGPA core which is low power. They designed using leakage memory cells, voltage scaling and Power gating to achieve low active and stand by Power [4]. Elif Bilge Kavun and Tolga Yalcin have proposed two different RAM based implementations of the lightweight cipher algorithm PRESENT on FPGAs. With their lowest reported slice counts, both implementations prove to be suitable for lightweight applications such as sensor nodes and RFIDs. While the first implementation uses slices for S-boxes, the second one integrates the S-boxes into the block RAM as well. This way, we provide two alternative platforms for future side channel attack (SCA) resistant implementations [6]. Willem Vereecken et.al proposed. some approaches on how to reduce this footprint and how ICT can assist in other sectors reducing their footprint. These strategies need to focus on reducing the power consumption but also reducing the complete life cycle impacts of the equipment. They described overview of the environmental issues related to communication technologies en present an estimation of the overall ICT footprint

[7]. Gaurav Verma et.al proposed some techniques for the low power design of digital systems using benchmark circuits. So, the authors have discussed some of the prominent techniques at each level. As seen the power minimization can be targeted at different levels of design hierarchy. The newer operating systems also include an ACPI module, so that the status of the device can be monitored and appropriate power management commands can be issued to save system power [9]. Pandey et.al have concluded that with increase in frequency, power dissipation also increases. DES algorithm is compatible with different WLAN frequencies, as we have analysed DES algorithm using four different WLAN frequencies (i.e. 2.4GHz, 3.6 GHz, 4.9 GHz and 5.9 GHz). As we have used 6 different IO Standards of category SSTL, from which we have concluded that SSTL135 and SSTL135_R are most efficient IO Standards for DES algorithm. They also observed that the leakage power dissipation is least for different on-chip components and IOs power is maximum. Therefore, energy efficient implementation of DES algorithm is possible with SSTL IOs Standards and different WLAN frequencies.
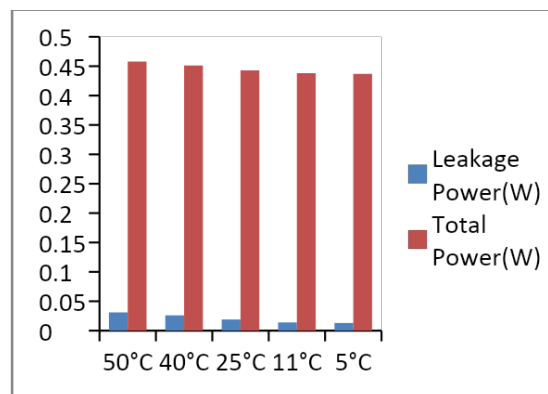
IV. POWER ESTIMATION AND RESULTS

A. POWER ESTIMATION OF ATM INTERFACED WITH SPARTAN 6 FGPA

When the Ambient temperature of Spartan 6 FGPA regulates from 50°C to 5°C , it is observed that there is only consumption of leakage power and all the other on chip power that is clocks, logic, I/O, signal are constant in discrete Ambient temperature when we changed in Spartan 6 FGPA or We can say Static Power changes but the dynamic power constant at each temperature in FGPA. As a temperature increases, there is an increase in leakage power. The Power chart of Spartan 6 FGPA as shown in Table 1.

Table 1. Leakage Power of Spartan 6 FGPA

| Temperature	Leakage Power(W)	Total Power(W)
50°C	0.031	0.458
40°C	0.026	0.451
25°C	0.019	0.443
11°C	0.014	0.438
5°C	0.013	0.437

Figure 2. Power V/S Voltage of Spartan 6 FGPA

B. POWER ESTIMATION OF ATM INTERFACED WITH VIRTEX 4 FGPA

When the Ambient temperature of Spartan 6 FGPA regulates from 50°C to 5°C, it is observed that there is only consumption of leakage power and all other parameters are negligible. As temperature decreases, the leakage power and total power also decreases. The Power chart of Virtex 4 FGPA as shown in Table 2.

Table 2. Leakage Power of Virtex 4 FGPA

Temperature(C)	Leakage Power(W)	Total Power(W)
50°C	0.173	0.496
40°C	0.160	0.483
25°C	0.143	0.467
11°C	0.131	0.454
5°C	0.127	0.450
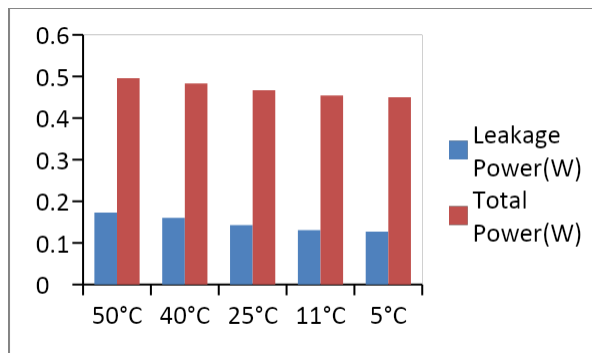
Figure 3. Power V/S Voltage of Virtex-4 FGPA

C. POWER ANALYSIS OF ATM INTERFACED WITH VIRTEX 4 FGPA VS SPARTAN 6 FGPA

As we comparing both we analysed that Spartan 6 FPGAs offer lower power, simpler power systems better reliability, and lower system cost. In table 3. At **50°C** Spartan 6 leakage power dissipation is low as compared to Virtex 6.

Table 3. Leakage Power Comparisions of Virtex 4 and Spartan 6

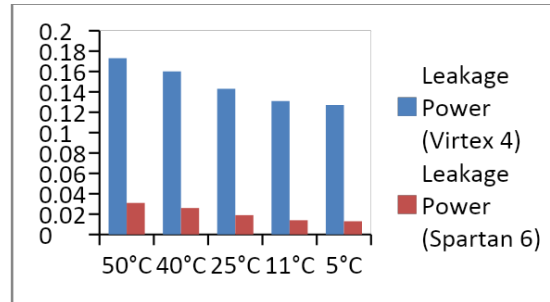| Temperature(C)	Leakage Power (Virtex 4)	Leakage Power (Spartan 6)
50°C	0.173	0.031
40°C	0.160	0.026
25°C	0.143	0.019
11°C	0.131	0.014
5°C	0.127	0.013

Figure 4. Comparison of leakage Power V/S Voltage of Spartan 6 FGPA

V. CONCLUSION

We interfaced our ATM Design with discrete FGPA families and trying to solve and has developed the low-cost, low-power FGPA family. We achieved thermal scaling by varying power and discrete Ambient temperature and also resolves the performance gap found between the Spartan 6 and   Virtex 4 FPGA using Leakage power. The leakage power reduction plays a key role in low power VLSI circuit designs. Hence Spartan 6 is more power- efficient device than Virtex 4 and most likely used in FGPA designing.   The integrated blocks in Spartan-6 FPGAs provide greater efficiency, ease-of-use, lower total power, lower cost, and adept connectivity and memory capabilities. Spartan-6 FPGA family extends its low-cost FPGA market leadership.

VI. FUTURE SCOPE

In future, newly emerging leakage power reduction techniques at block level and gate level abstractions are expected to give more power savings than the existing circuit level techniques and also Power and Energy reduction and recycling will continue to be dominant topics for the foreseeable future. We can also interface Automated teller machine with other FGPA families like Kintex 7, Zynq, Artix 7 etc for analysing a power. We can also scale the voltage value, frequency value and change I/O standards to observe the variation in the power consumption that will be helpful in green communication.

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