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Wrist Band Design using Low Power Virtex6 FPGA for Monitoring Blood Pressure

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***Abstract*— Out of control blood pressure whether it is low or high can be dangerous and major cause of heart disease. The people suffering from blood pressure problems are increasing day by day. The main objective of this paper is to make a wrist band which can monitor the blood pressure of our body at any time. The approach is to make it consume low power for its operation. Technique applied for doing same is capacitance scaling using Field Programmable gate Array using Xilinx software. The power consumption at frequency 0.2GHz, 1GHz, 2GHz, 20GHz and 200GHz is calculated for Low PowerVirtex6 FPGA.**

Keywords- *Blood Pressure, Power Consumption, FPGA, Capacitance Scaling, Frequency*

I. INTRODUCTION

According to Global Health Observatory i.e. GHO data it is observed that almost 7.5 million deaths are due to hypertension i.e. high blood pressure [1]. This approximates to about 12.8% of the total deaths and is large value. Hypertension increases the risk of major heart diseases. It is very important to monitor the blood pressure and treat the problem at early stage. The statics of raised blood pressure is shown in Fig1.

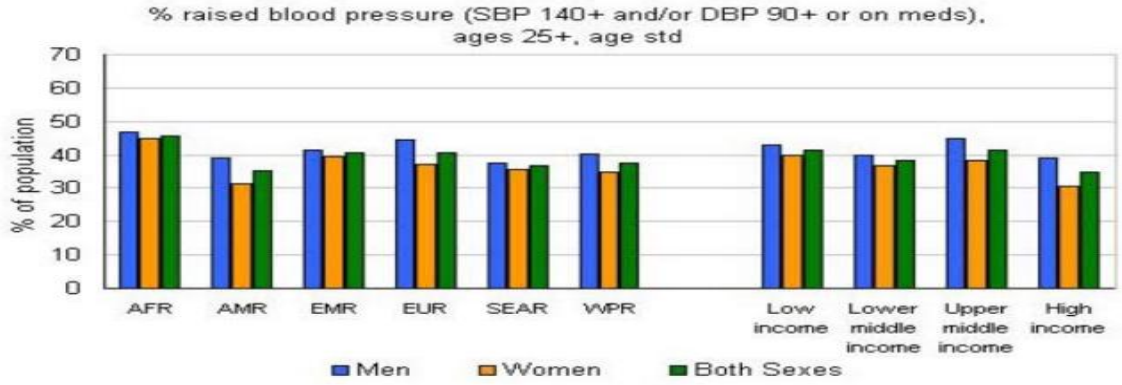

Fig1: Percentage raised Blood Pressure in adults for different regions.

Blood Pressure is defined as the pressure exerted by blood on the walls of arteries and veins, when blood flows through them. It is exerted when blood is pumped by the heart into blood vessels. It is measured in millimeters of mercury i.e. mm Hg. Normal blood pressure range is 120/80 to 140/90 where 120-140 is Systolic mm Hg and 80-90 is Diastolic mm Hg. Systolic means the pressure exerted when the heart is beating and Diastolic means when heart is resting between the beats. If the blood pressure is above normal range it is known as high blood pressure and also called Hypertension. And if it is less than normal range is low blood pressure also known as Hypotension. The different stages for different values of blood pressure are explained below and shown in Fig2.

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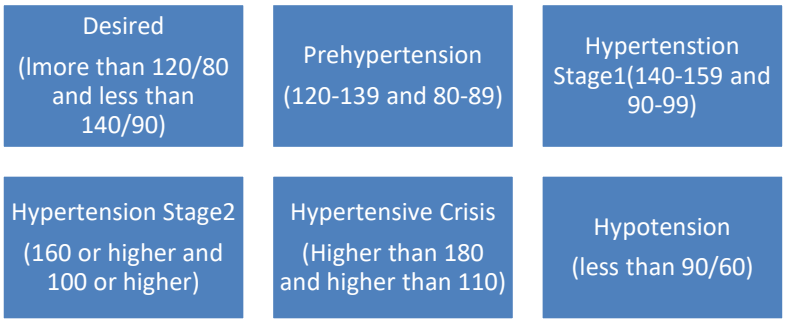

Fig2: Different Stages at different values of Blood Pressure both systolic and diastolic mm Hg

Wrist Band is a device which is used to monitor the blood pressure of human body and is extremely sensitive to position of the body. It is a useful device which can ensure about your blood pressure at any instant of time. In this project wrist band is analyzed using Xilinx. It is need of the hour to control the power consumption as resources of energy are limited for future use. So approach is to present a band which consumes less power and is efficient device. Capacitance Scaling is done for the attaining the same at different frequencies. Low Power Virtex6 FPGA is used for LVDCI_25 Standard. The RTL Schematic view of wrist band is shown in Fig3.

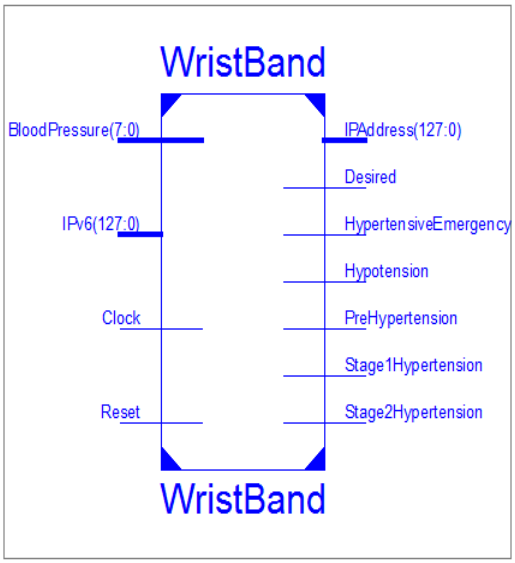

Fig 3: Schematic View of Wrist Band

II. RELATED WORK

In this column we are relating the work that has already been done in this area and how that work is different from our paper. There are a lot of wrist bands available in market but very less work is done to make these bands energy efficient. We have used capacitance scaling to obtain least amount of power for operation of the band. Some of the related papers are:

1. **Blood pressure monitoring system [2]**
   This is a blood Pressure Monitor System in which the analog waveforms are converted to digital form and are obtained using wrist mounted transducer. The idea is same to make the blood pressure monitoring system but approach is completely different. We have used FPGA for making the device and energy conservation factor is also a additional feature introduced in our work.

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2. **Portable blood pressure measuring device and method of measuring blood pressure [3]**
   In this paper also transducer is used to convert the output signals to systolic and diastolic readings .The blood pressure can be checked at any instant of time as same our device. This paper also lacks the energy efficient Scheme. No work is done to make it consume less power.
3. **Occlusive non-inflatable blood pressure device [4]**
   This device is placed around the limb and contains compressible material. This device is not similar wrist band and is used to check the blood pressure at particular time only. This design is totally different as our design is made using Field Programmable Gate Array for the purpose of saving energy consumption of the device using LVDCI_25 standard.
4. **A CMOS-Based Tactile Sensor for Continuous Blood Pressure Monitoring [5]**
   This system provides the better readings of blood pressure data due to capability of recording continuous data. It is fabricated using CMOS technology and changes in capacitance are detected by modulator which is operating at a sampling rate of 128kS/s. This paper is quite similar to our as the technology used is CMOS.
   There are many other papers that work for saving the energy consumption by using different scaling techniques and have similar approach i.e. multiplier based on HSTL IO Standard [6], DES Algorithm Design [7] and Arithmetic Logic Unit Design on 28nm FPGA using SSTL [8] .

III. DATA EXAMINATION AND RENDERING

1. Result For 0.2GHz

Table 1: Readings of Clock, Logic, Signal, I/O , Leakage and Total Power at 0.2GHz

Output Load	5pF	50pF	100pF	150pF	200pF
Clock	0.002	0.002	0.002	0.002	0.002
Logic	0.000	0.000	0.000	0.000	0.000
Signal	0.000	0.000	0.000	0.000	0.000
I/O	0.117	0.132	0.148	0.165	0.181
Leakage	0.486	0.487	0.487	0.487	0.487
Total Power	0.606	0.621	0.638	0.655	0.671

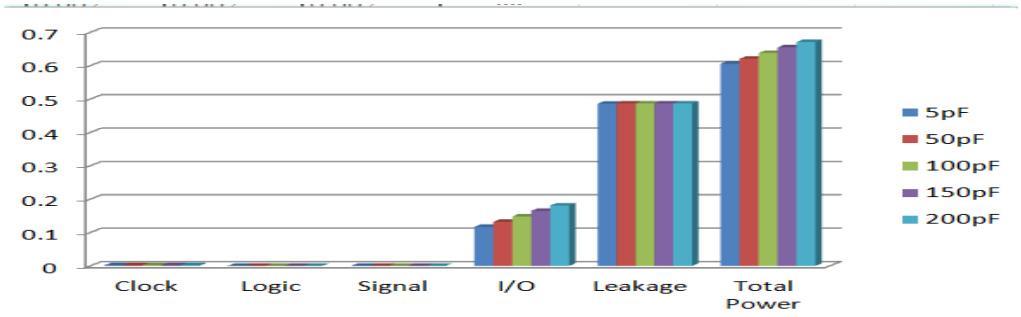

Fig 4: Graph of Clock, Logic, Signal, I/O , Leakage and Total Power at 0.2 GHz

Clock, Logic and signal don't show any change in their values even after scaling capacitance from 5pF to 200pF at 0.2GHz. There is slight change in Leakage is about 0.2% when

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capacitance is scaled form 50pF to 5pF. Percentage curtail in I/O is 8.8%, 18.23%, 27.07% and 35.35% when capacitance is scaled down from 200pF to 150pF, 100pF, 50pF and 5pF respectively. Percentage curtail in overall power consumed is 2.38%, 4.91%, 7.45% and 9.68% when capacitance is scaled down from 200pF to 150pF, 100pF, 50pF and 5pF respectively as shown in Fig 4.

2. Result For 1GHz

Table 2: Readings of Clock, Logic, Signal, I/O , Leakage and Total Power at 1GHz

Output Load	5pF	50pF	100pF	150pF	200pF
Clock	0.012	0.012	0.012	0.012	0.012
Logic	0.000	0.000	0.000	0.000	0.000
Signal	0.001	0.001	0.001	0.001	0.001
I/O	0.277	0.595	0.949	1.303	1.656
Leakage	0.489	0.494	0.499	0.504	0.510
Total Power	0.780	1.102	1.461	1.820	2.179

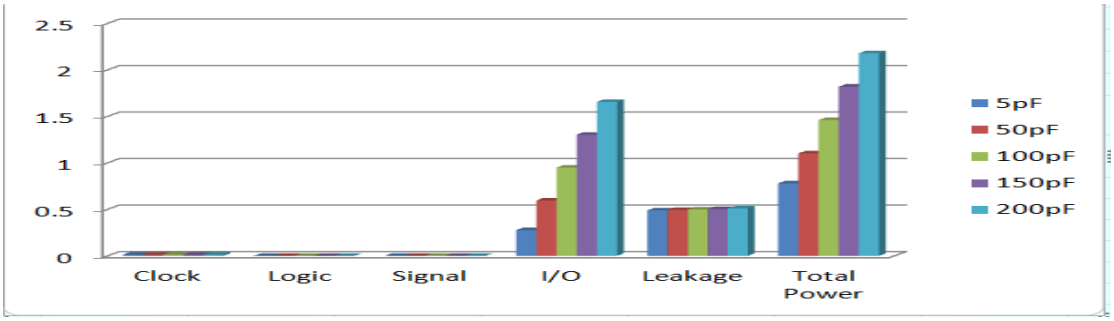

Fig 5: Graph of Clock, Logic, Signal, I/O , Leakage and Total Power at 1GHz

Clock, Logic and signal don't show any change in their values even after scaling capacitance from 5pF to 200pF at 0.2GHz. Percentage curtail in I/O is 2.13%, 4.26%, 6.40% and 83.27% when capacitance is scaled down from 200pF to 150pF, 100pF, 50pF and 5pF respectively. Percentage curtail in Leakage is 1.17%, 2.156%, 3.13% and 4.11% when capacitance is scaled down from 200pF to 150pF, 100pF, 50pF and 5pF respectively. Percentage curtail in overall power consumed is 1.64%, 3.29%, 4.94% and 6.42% when capacitance is scaled down from 200pF to 150pF, 100pF, 50pF and 5pF respectively as shown in Fig 5.

3. Result For 2GHz

Table 3: Readings of Clock, Logic, Signal, I/O , Leakage and Total Power at 2GHz

Output Load	5pF	50pF	100pF	150pF	200pF
Clock	0.024	0.024	0.024	0.024	0.024
Logic	0.000	0.000	0.000	0.000	0.000
Signal	0.002	0.002	0.002	0.002	0.002
I/O	0.764	2.011	3.396	4.781	6.166
Leakage	0.496	0.516	0.538	0.562	0.587
Total Power	1.287	2.553	3.961	5.370	6.780

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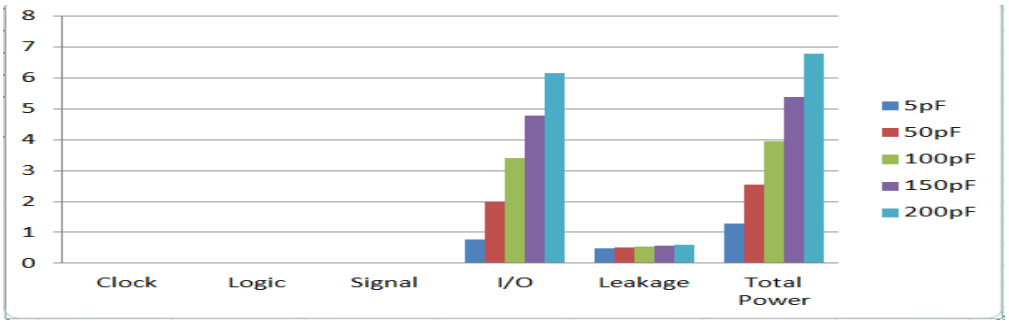

Fig 6: Graph of Clock, Logic, Signal, I/O , Leakage and Total Power at 2GHz

Clock, Logic and signal don't show any change in their values even after scaling capacitance from 5pF to 200pF at 0.2GHz. Percentage curtail in I/O is 22.46%, 44.92%, 67.38% and 87.60% when capacitance is scaled down from 200pF to 150pF, 100pF, 50pF and 5pF respectively. Percentage curtail in Leakage is 4.25%, 8.34%, 12.09% and 15.50% when capacitance is scaled down from 200pF to 150pF, 100pF, 50pF and 5pF respectively. Percentage curtail in overall power consumed is 21.68%, 41.57%, 62.34% and 81.01% when capacitance is scaled down from 200pF to 150pF, 100pF, 50pF and 5pF respectively as shown in Fig 6.

4. Result For 20GHz (0.05ns)

Table 4: Readings of Clock, Logic, Signal, I/O , Leakage and Total Power at 20GHz

Output Load	5pF	50pF	100pF	150pF	200pF
Clock	0.241	0.241	0.241	0.241	0.241
Logic	0.002	0.002	0.002	0.002	0.002
Signal	0.018	0.018	0.018	0.018	0.018
I/O	9.598	27.688	47.787	67.886	87.986
Leakage	0.661	0.689	0.689	0.689	0.689
Total Power	10.519	28.637	48.736	68.836	88.935

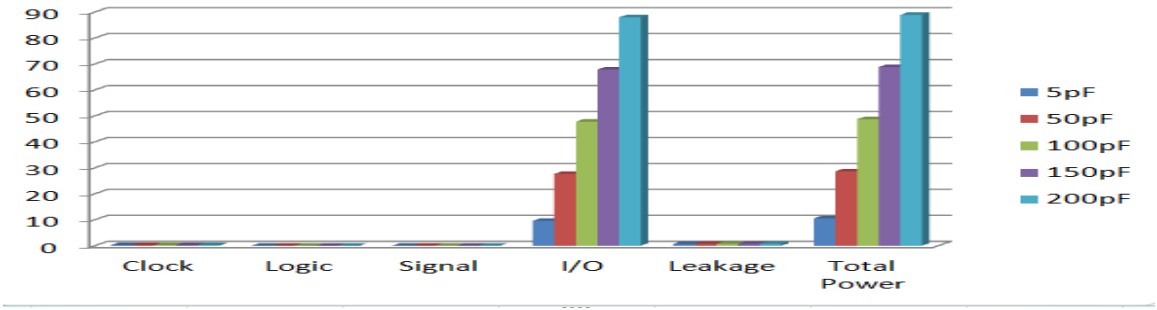

Fig 7: Graph of Clock, Logic, Signal, I/O , Leakage and Total Power at 20GHz

Clock, Logic and signal don't show any change in their values even after scaling capacitance from 5pF to 200pF at 0.2GHz.
There is slight change in Leakage is about 4.06% when capacitance is scaled form 50pF to 5pF.
Percentage curtail in I/O is 22.84%, 45.68%, 68.53% and 99.32% when capacitance is scaled down from 200pF to 150pF, 100pF, 50pF and 5pF respectively.

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Percentage curtail in overall power consumed is 22.59%, 45.20%, 67.80% and 88.17% when capacitance is scaled down from 200pF to 150pF, 100pF, 50pF and 5pF respectively as shown in Fig 7.

5. Result For 200GHz

Table 5: Readings of Clock, Logic, Signal, I/O , Leakage and Total Power at 200GHz

Output Load	5pF	50pF	100pF	150pF	200pF
Clock	2.406	2.406	2.406	2.406	2.406
Logic	0.002	0.002	0.002	0.002	0.002
Signal	0.156	0.156	0.156	0.156	0.156
I/O	111.505	323.997	560.098	796.199	1032.301
Leakage	0.0689	0.689	0.689	0.689	0.689
Total Power	114.758	327.249	563.351	799.452	1035.554

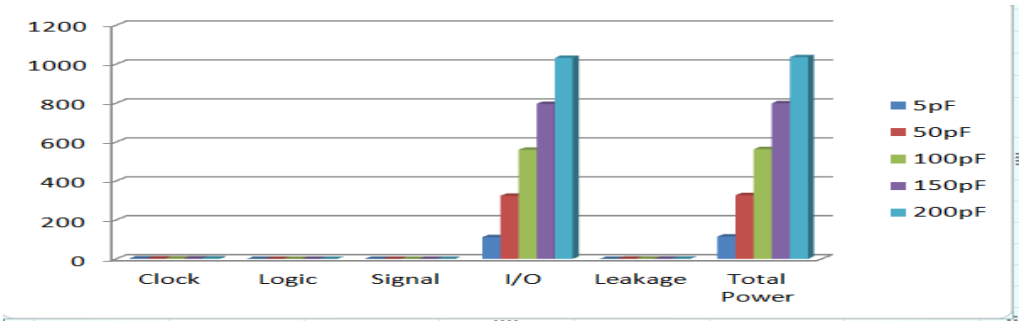

Fig 8 : Graph of Clock, Logic, Signal, I/O , Leakage and Total Power at 200GHz

Clock, Logic, signal and Leakage don't show any change in their values even after scaling capacitance from 5pF to 200pF at 0.2GHz.
Percentage curtail in I/O is 22.87%, 45.74%, 68.61% and 89.19% when capacitance is scaled down from 200pF to 150pF, 100pF, 50pF and 5pF respectively.
Percentage curtail in overall power consumed is 22.79%, 45.59%, 68.39% and 88.91% when capacitance is scaled down from 200pF to 150pF, 100pF, 50pF and 5pF respectively as shown in Fig 8.

IV. CONCLUSION

Wrist band is a useful device that can contribute to diagnose heart diseases due to fluctuations in blood pressure. The work is successfully done to make this device energy efficient by the approach of varying output load at different frequencies. Total Percentage Curtail in total Power consumed observed is 88.91% at frequency 200 GHz and for I/O maximum reduction is 99.32% at 20Hz. So, it can be concluded that there is noticeable change by varying output load at different value of frequency using low power Virtex-6 FPGA.

V. FUTURESCOPE

Blood Pressure fluctuations are the major problem faced by millions of people today and lead to major diseases. Firstly diagnose is more important than curing the problems at later stages. So this device can help people know about how usually their blood pressure fluctuates. This device will be energy efficient and hence saves energy. In future different approaches can be

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made to attain the same or better than this. Different FPGA families like Kintex-7, Airtex-7 etc. can be used for different standards like HSTL, LVCMOS, SSTL and PCI33_3 [9] etc. Frequency Scaling can also be done in future instead of varying the output load.

REFERENCES

[1] WHO data available at: http://www.who.int/gho/ncd/risk_factors/blood_pressure_prevalence_text/en/
[2] Barnes, Jeffrey T., and J. Erik Moore. "Blood pressure monitoring system." U.S. Patent 5,406,952, issued April 18, 1995.
[3] Jackson, R. Sandra, and H. E. Jackson. "Portable blood pressure measuring device and method of measuring blood pressure." U.S. Patent No. 5,485,848. 23 Jan. 1996.
[4] Welch, P. James, B. S. Long. "Occlusive non-inflatable blood pressure device." U.S. Patent Application No. 13/565,691.
[5] Kirstein, K-U., et al. "A CMOS-based tactile sensor for continuous blood pressure monitoring." IEEE Computer Society, 2005.
[6] S. Madhok , B. Pandey and A. Kaur , M. H. Minver and D. M. A. Hussain, “HSTL IO Standard Based Energy Efficient Multiplier Design using Nikhilam Navatashcaramam Dashatah on 28nm FPGA”, International Journal of Control and Automation Vol.8, No.8 , pp.35-44,2015
[7] V. Thind, B. Pandey, K. Kalia, D M A. Hussain, T. Das and T. Kumar, “FPGA Based Low Power DES Algorithm Design and Implementation using HTML Technology”, International Journal of Software Engineering and Its Applications Vol. 10, No. 6 pp. 81-92,2016
[8] K. Kalia, B. Pandey, T. Das, D M A. Hussain, “SSTL Based Low Power Thermal Efficient WLAN Specific 32bit ALU Design on 28nm FPGA”, Indian Journal of Science and Technology, Vol.9, No.10, March 2016. http://www.indjst.org/index.php/indjst/article/view/88080
[9] D. Singh, K. Garg, R.Singh, B. Pandey, K.Kalia, and H. Noori. "Thermal aware Internet of Things Enable Energy Efficient Encoder Design for security on FPGA." International Journal of Security and Its Applications 9, no. 6, June 2015, Page: 271-278.