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Low Power Design of Video PHY Controller (2.0) for HDMI Protocol Using Unidirectional High Performance IO Standard

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Abstract— **The Video PHY controller is an important device that provides the interface between Transceivers and video interfaces. This interface either is HDMI or Displayport. HDMI Video PHY controller are more significantly used because they provide the high speed operation for high resolution graphics. However, when high resolution graphics are executed the power consumption of HDMI Video PHY controller becomes critical and this disturb the regular streaming of video or even in some cases may damage the HDMI Video PHY controller. There are various techniques have been adopted but significantly results in power reduction of HDMI Video PHY controller not been achieved. In this paper, the low power design for HDMI Video PHY controller is achieved using unidirectional IO Standard. It is demonstrated that POD IO Standard consumes less power for LVDCI IO Standard. The IO Standard based HDMI Video PHY controller is verified on high frequencies of 2.0 GHz and 6 GHz for providing the maximum line rate of 6 Gb/s. It is determined that power reduction of 51% is accomplished for HDMI based Video using unidirectional POD IO Standard compared to LVDCI IO Standard for 2 GHz operation. For 6 GHz GHz design of HDMI based Video PHY controller the power reduction of 73% is achieved using POD IO Standard compared to LVDCI IO Standard. The proposed design will be to provide high resolution graphics at low power consumption.**

***Keywords- Power Consumption, Video PHY Controller, IO Standard, UltraScale Field Prograaming Gate Array*.**

I. INTRODUCTION

The Video PHY controller is used to configure, the PHY layer with video MAC controllers. The PHY layer streamline the usage of serial transceivers configurability. The Video PHY offers the rigidity of allocation for GTH Transceivers between a video interfaces. This is allocation is reserved for video interface I/O or between video interfaces such as; HDMI and Displayport [1]. However, it is very much important to investigate the behavior, power consumption, usage, and any limitations of the Video PHY controller. For HDMI, the Video PHY controller consumes an enormous power as it works on high frequencies of 2.0 GHz to 6.25 GHz for providing the maximum line rate of 6 Gb/s [1]. It has been observed that for high resolution video process using HDMI Port. The power consumption of Video PHY controller is also increasing [2]. There are several techniques are utilized in order to control or reduce the power consumption of different devices such as; optical transmitter [3], energy efficient laser driver [4], Ethernet [5], filters [6]. These techniques include; these techniques include; clock gating, voltage scaling [7], variable frequency and etc. However, each techniques has its own advantages and disadvantages. It has been demonstrated in [8-9] that for different variation in suitable IO Standard the power consumption of device can be reduced depend upon the core voltage of Field Programming Gate Array (FPGA), operating voltage of the device and IO Standard voltage selected for particular device. In this paper, the

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low power consumption is demonstrated for HDMI based Video PHY controller for high frequency using IO Standard via UltraScale Field Programming Gate Array. The Unidirectional IO Standard is selected based on the criteria of core voltage of FPGA, and operating voltage of HDMI based Video PHY controller.

II. METHODOLOGY

The low power HDMI based Video PHY controller for high frequency using IO Standard is designed using different design steps as demonstrated in Figure 1. It is illustrated in Figure 1 that in first design step, the HDMI based Video PHY controller is designed using Vivado design suite via vhdl coding by defining the different parameters and configuration of transmitter and receiver. In the second design step, the vhdl based HDMI based Video PHY controller is designed using IO Standard. The IO Standard is selected based upon the core voltage of FPGA, and operating voltage of HDMI based Video PHY controller. In the third design step, the vhdl based HDMI Video PHY controller using unidirectional IO Standard is tested for different high frequencies in order to analyze the performance of the designed low power HDMI based Video PHY controller. In the last step, the IO Standard that consumes less power for HDMI based Video PHY controller is considered as low power design of HDMI based Video PHY controller.

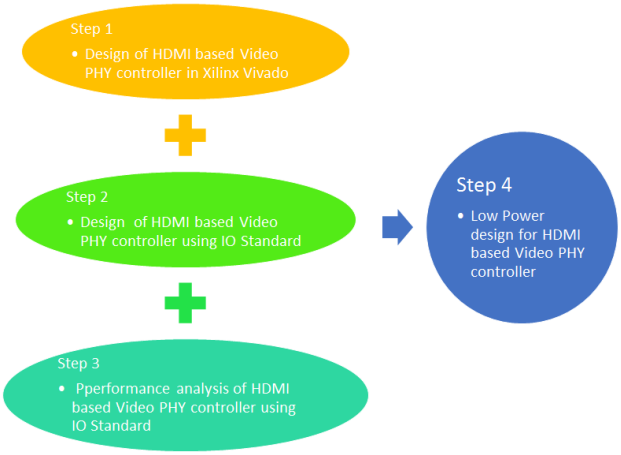

Figure 1. Design steps to developing the low power design for HDMI based Video PHY controller

A. Design Step 1: vhdl based HDMI based Video PHY controller

The HDMI based Video PHY controller is designed in Xilinx Vivado Suite using vhdl. The elaborated/schematic design of Video PHY controller is shown in Figure 2.

Figure 2. Schematic design of Video PHY controller

The Video PHY controller in Figure 2 is designed using different protocols parameters as illustrated in Table 1.

Table 1. Protocol parameters for HDMI based Video PHY controller

NAME OF PARAMETER	PARAMETER CONFIGURATION
Tx Protocol	HDMI
Tx Max GT line rate	6.4 Gb/s
Tx channels	3
Tx PLL type	QPLL 0/1
Tx Ref Clock	GTREFCLK1
Rx Protocol	HDMI
Rx Max GT line rate	6.4 Gb/s
Rx channels	3
Rx PLL type	CPLL
Rx Ref Clock	GTREFCLK0
No of pixels per clock	6
Clock Frequency	100 MHz

Table 1 describes the different protocols parameters for HDMI based Video PHY controller. The interface for the Video controller is HDMI. The maximum line is 6.4 Gb/s using Phase Locked Loop (PLL) configuration. In the Schematic of HDMI based Video PHY controller there are three channels are selected for transmission and three channel are selected for receiver. There different clock signals are utilized to synchronize the transmitter and receiver data rate. It can be analyzed in Figure 2 that two pins are left named because these are configured to design the IO Standard for Video PHY controller. The IO Standard design of Video PHY controller is demonstrated in the next section.

B. Design Step 2: IO Standard based HDMI based Video PHY controller

In UltraScale FPGA an I/O tile is defined with I/O buffers, I/O logics and I/O delays. Each IOB contains both input and output logic and IO drivers. These drivers can be configured to various I/O standards [9]. The IO Standard based schematic diagram of HDMI based Video

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PHY controller is demonstrated using Figure 3. It is defined in Figure 3 that device configuration has been changed by adding the IO Standard and its related operating voltage in VHLD based HDMI based Video PHY controller.

Figure 3. Schematic design of IO based 10G Ethernet Media Access Controller

Virtex UltraScale FPGA support many IO Standard a long list is available in [9]. In this research, authors have selected the unidirectional IO Standards that meet the requirements for HDMI based Video PHY controller. These IO Standards are specified in the Electronic Industry Alliance JEDEC [10]. The reason for selecting the unidirectional IO Standard for HDMI based Video PHY controller is that unidirectional offers the program in simple mode without handshaking, and second the unidirectional IO Standards offers the High Performance (HP) IO Standard that suitable for HDMI based Video PHY controller, Because fir high frequency, the process of cycling number of pixels for HDMI interface need a HP for better resolution of HDMI port. There are different types of unidirectional IO Standards are available such as; Low Voltage Transistor Transistor Logic (LVTTL), Low Voltage Complementary Metal-Oxide Semiconductor (LVCMOS), Low-Voltage Digitally Controlled Impedance (LVDCI), High-Speed Low-Voltage Digitally Controlled Impedance (HSLVDCI), High-Speed Transceiver Logic (HSTL), High Speed Unterminated Logic (HSUL), Pseudo Open Drain (POD) and many more. These unidirectional IO Standards are further divided in High Range (HR) and High Performance (HP) category. It is already discussed in above discussion that for HDMI based Video PHY controller, the HP IO Standard are required in order to process the pixels at faster rate. The above unidirectional IO Standards are categorized as; LVTTL is HR IO Standard, LVCMOS is HR and HP both Standard, LVDCI is HP IO Standard, HSLVDCI is HP IO Standard, HSTL is HR IO Standard, HSUL) is both HR and HP IO Standard, and POD is HP IO Standard. It is defined that for HDMI based Video PHY controller that LVDCI IO Standard and POD IO Standard are selected for low power design. The reason for choosing these HP IO Standard from several other unidirectional IO Standard is that both LVDCI and POD has low termination impendence with low reference of 1.0 V to 1.8 V. In the next section, both LVDCI and POD are discussed.

1) *Low-Voltage Digitally Controlled Impedance (LVDCI) IO Standard*

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LVDCI is used to control the impedance drivers. The LVDCI provides the controlled impedance output driver to provide series termination without external source termination resistors. It offers the valid value of this attribute for LVDCI IO Standard standards is RDRV_48_48, which corresponds to a 48Ω. The LVDCI supports the LVDCI_15 and LVDCI_18. LVDCI offers the reference voltage of 1.5V and 1.8 respectively for LVDCI_15 and LVDCI_18 [11]. The syntax for changing the IO Standards from default to user defined IO Standards (LVDCI) is:

a)

attribute IOSTANDARD : string;

attribute IOSTANDARD of IDIOA0 : label is- "LVDCI_15";

b)

attribute IOSTANDARD : string;

attribute IOSTANDARD of IDIOA0 : label is- "LVDCI_18";

2) Pseudo Open Drain (POD) IO Stadard

Pseudo Open Drain (POD) standards are planned for DDR4, DDR4L, and LLDRAM3 applications that provides the high performance. The Pod supports the POD12 and POD10 IO Standards as unidirectional board topology for POD with reference voltage of 1.0V and 1.2V respectively for POD12 and POD12 with matched driver and receiver termination values. POD corresponds to 45Ω termination impedance for the devices. The syntax for changing the IO Standards from default to user defined IO Standards (POD) is:

a)

attribute IOSTANDARD : string;

attribute IOSTANDARD of IDIOA0 : label is- "LVDCI_15";

b)

attribute IOSTANDARD : string;

attribute IOSTANDARD of IDIOA0 : label is- "LVDCI_18";

C. Design Step 3: Performance Analysis of IO Standard based HDMI based Video PHY controller using power analysis

The performance of IO Standard based HDMI Video PHY controller is analyzed for high frequency operation of 2 GHZ and 6 GHz. The power analysis is performed for these high frequencies using LVDCI and POD Standards as discussed earlier for IO Standard based HDMI Video PHY controller.

The power analysis for based HDMI Video PHY controller in UltraScale FPGA power is comprises of sum of device static power, design static power and design dynamic power presented in equation (1) [9].

$$Total\ FPGA\ power = Design\ Dynamic\ Power + Device\ Static\ Power + Design\ Static\ Power \quad (1)$$

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Device static power characterizes the transistor leakage power when devices is powered and not configured. Design Dynamic power epitomizes the power associated with design activity and switching events in the core or I/O of the device. Dynamic power is determined by node capacitance, supply voltage, and switching frequency. Design static power denotes the power consumption when the device is configured with no switching activates. The power consume by clock manager.

1) Performance Analysis of IO Standard based HDMI Video PHY controller for 2 GHz frequency via LVDCI IO Standard

The performance of the HDMI based Video PHY controller is analyzed for 2 GHz for LVDCI IO Standard by measuring the on-chip power. The LVDCI is configured for the reference voltage of 1.5 V. Therefore the LVDCI syntax will be changed to LVDCI_15.The on chip power is measured in terms of dynamic power. Figure 4 defines the on-chip power analysis for 2 GHz at LVDCI_15 IO Standard for HDMI based Video PHY controller.

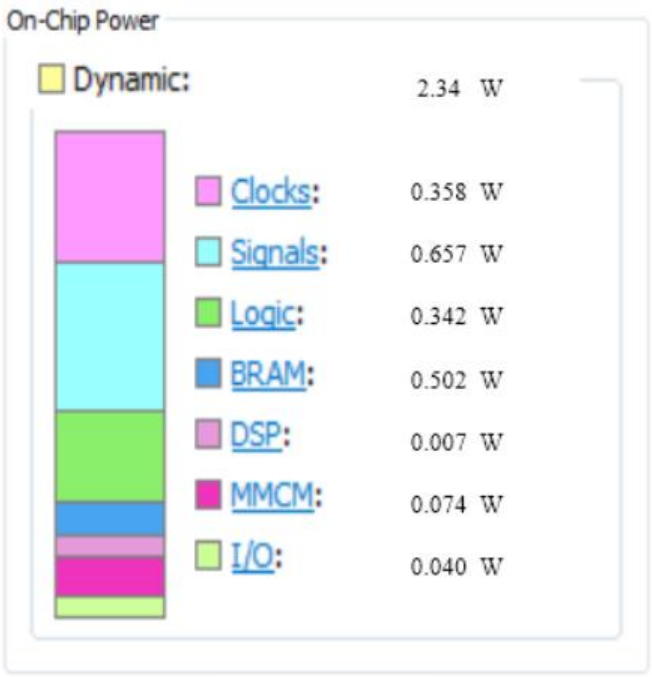

Figure 4. On- Chip Power measurement for HDMI based Video PHY controller at 2 GHz for LVDCI_15 IO Standard

It can be analyzed from Figure 4 that 2.34 W dynamic power is consumed by HDMI based Video PHY controller. IO power consumed is 0.04 W. The most of the power is consumed by signal and BRAM power. It is also important to note that although LVDCI has low reference voltage and low termination impedance for high performance application the RAM power is consumption is more.

2) Performance Analysis of IO Standard based HDMI Video PHY controller for 6 GHz frequency via LVDCI IO Standard

The performance of the HDMI based Video PHY controller is analyzed for 6 GHz for LVDCI IO Standard by calculating the on-chip power. The LVDCI is configured syntax is

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changed to LVDCI_15. Figure 5 defines the on-chip power analysis for 6 GHz at LVDCI_15 IO Standard for HDMI based Video PHY controller. It can be analyzed from Figure 5 that 4.422 W dynamic power is consumed by HDMI based Video PHY controller, the IO power consumed is 0.520 W. The most of the power is consumed by signal and BRAM power.

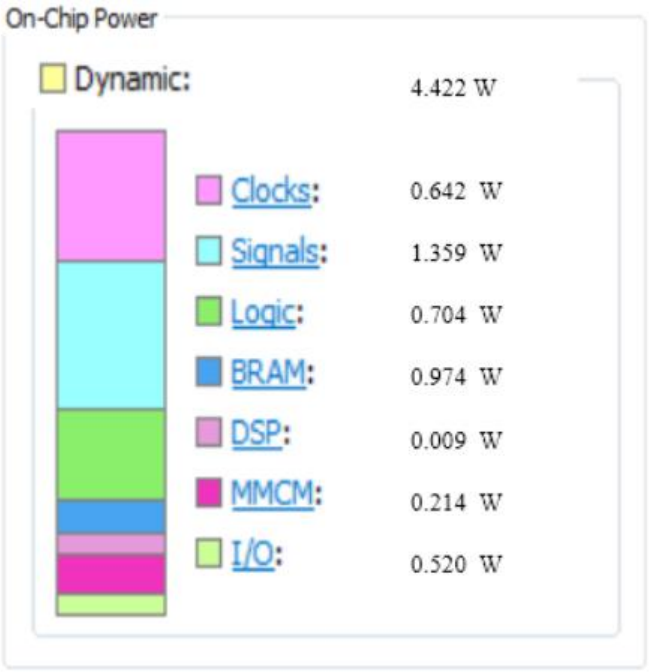

Figure 5. On- Chip Power measurement for HDMI based Video PHY controller at 6 GHz for LVDCI_15 IO Standard

It can be observed from Figure 5 that dynamic power consumed by HDMI based Video PHY controller is 4.422 W. It can analyzed that IO power is significantly is increased to 92 %. It is also defined that signal power is also increased compared to HDMI based Video PHY controller designed at 2 GHz for LVDCI_15 IO Standard.

3) Performance Analysis of IO Standard based HDMI Video PHY controller for 2 GHz frequency via POD IO Standard

The performance of the HDMI based Video PHY controller is analyzed for 2 GHz for POD IO Standard by measuring the on-chip power. The POD is configured for the reference voltage of 1.0 V. Therefore the LVDCI syntax will be changed to POD_10.The on chip power is measured in terms of dynamic power. Figure 6 defines the on-chip power analysis for 2 GHz at POD_10 IO Standard for HDMI based Video PHY controller. It can be analyzed from Figure 6 that 1.144 W dynamic power is consumed by HDMI based Video PHY controller. IO power consumed is 0.012 W. The most of the power is consumed by signal and logic power. Here, it is important to note that POD_10 IO Standard is consuming less signal and BRAM compared to LVDCI_15 for HDMI based Video PHY controller, when operated at 2 GHz. The POD IO Standard offers the high performance application for high resolution of HDMI based Video PHY controller. POD offers the DDR4 high speed bus operation for HDMI based Video PHY controller.

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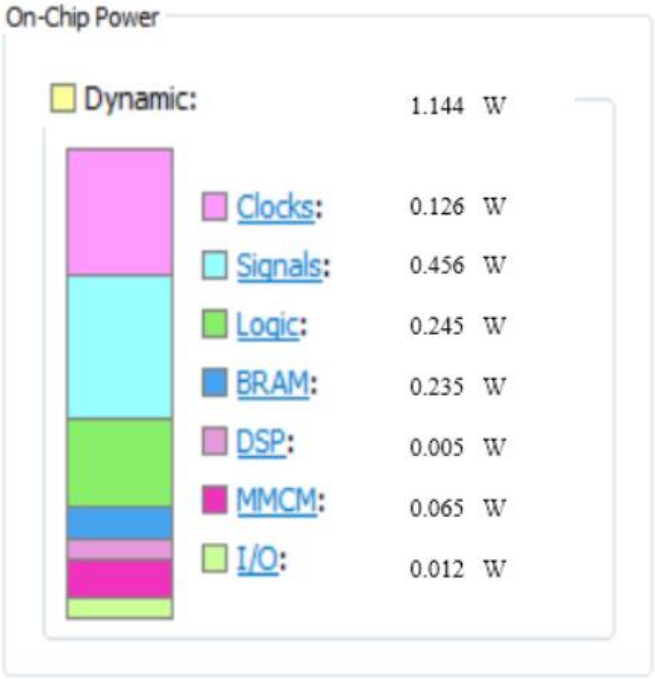

Figure 6. On- Chip Power measurement for HDMI based Video PHY controller at 2 GHz for POD_10 IO Standard

It is defined that signal power is reduced to 30% for POD_10 IO Standard for 2 GHz operation of HDMI based Video PHY controller compared to LVDCI_15 IO Standard for 2 GHz operation of HDMI based Video PHY controller. Similarly, the BRAM power is reduced 53%, for POD_10 IO Standard for 2 GHz operation of HDMI based Video PHY controller compared to LVDCI_15 IO Standard for 2 GHz operation of HDMI based Video PHY controller. Correspondingly, the IO Power reduction is observed up to 70% for POD_10 IO Standard for 2 GHz operation of HDMI based Video PHY controller compared to LVDCI_15 IO Standard for 2 GHz operation of HDMI based Video PHY controller. It is determined that when HDMI based Video PHY controller is operated at 2 GHz for POD IO Standard significant power reduction is achieved compared to HDMI based Video PHY controller is operated at 2 GHz for LVDCI IO Standard. In the next, the frequency has been increased from 2 GHz to 6 GHz for HDMI based Video PHY controller. The power analysis is analyzed for both LVDCI and POD Io Standard.

4) Performance Analysis of IO Standard based HDMI Video PHY controller for 6 GHz frequency via POD IO Standard

The dynamic power of the HDMI based Video PHY controller for 6 GHz via LVDCI_15 IO standard is demonstrated in Figure 7. The performance of the HDMI based Video PHY controller is analyzed for 6 GHz for POD IO Standard by computing the on-chip power. The POD is configured and syntax is changed to POD_10. It is demonstrated in Figure 7 that on-chip power analysis for HDMI based Video PHY controller at 6 GHz for POD_10 IO Standard is 1.669 W. The IO power consumed by HDMI based Video PHY controller is 0.099 W. The most of the power is consumed by logic and signal power. It has been observed that POD_10 IO Standard is consuming less signal and BRAM compared to LVDCI_15 for HDMI based Video PHY controller, when operated at 6 GHz.

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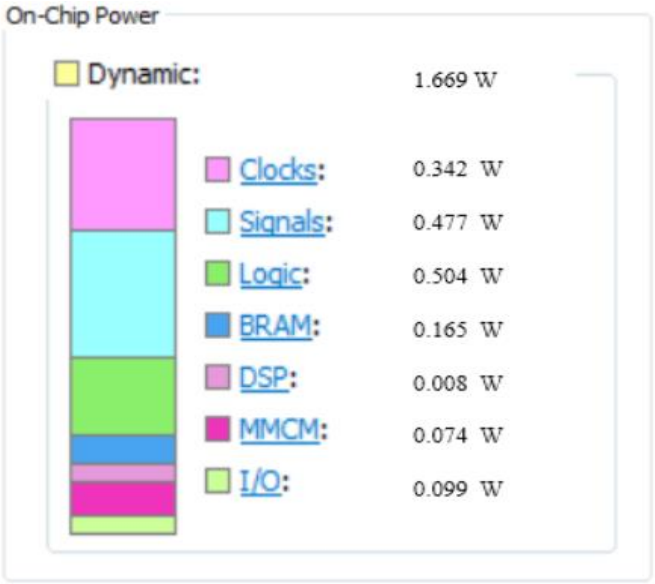

Figure 7. On- Chip Power measurement for HDMI based Video PHY controller at 6 GHz for POD_10 IO Standard

It has been analyzed that signal power is reduced to 64% for POD_10 IO Standard for 6 GHz operation of HDMI based Video PHY controller compared to LVDCI_15 IO Standard for 6 GHz operation of HDMI based Video PHY controller. Similarly, the BRAM power is reduced 83%, for POD_10 IO Standard for 6 GHz operation of HDMI based Video PHY controller compared to LVDCI_15 IO Standard for 6 GHz operation of HDMI based Video PHY controller. Similarly, the IO Power reduction is observed up to 80% for POD_10 IO Standard for 6 GHz operation of HDMI based Video PHY controller compared to LVDCI_15 IO Standard for 6 GHz operation of HDMI based Video PHY controller. It is illustrated that when HDMI based Video PHY controller is operated at 6 GHz for POD IO Standard significant power reduction is achieved compared to HDMI based Video PHY controller is operated at 6 GHz for LVDCI IO Standard. In this section, the power analysis is discussed. In the next, the results are discussed for proposed low power design for HDMI based Video PHY controller. It has been analyzed that proper selection of IO Standards may yield reduction in power consumption.

III. RESULTS AND DISCUSSION

In this paper, low power design for HDMI based Video PHY controller is proposed using unidirectional IO Standard. The IO Standard are selected according to specification of for HDMI based Video PHY controller and UltraScale FPGA. It is determined that for HDMI based Video PHY controller is tested for 2 GHz and 6 GHz using LVDCI_15 and POD_10 IO Standard. It is illustrated that when, for HDMI based Video PHY controller is operated at 2 GHz for LVDCI_15 the total dynamic power was 2.34 W. This dynamic power is compared with design of 2 GHz of for HDMI based Video PHY controller using POD_10 IO Standard, which is 1.144 W. It can be observed that POD_10 IO Standard is fully capable to reduce the power consumption for HDMI based Video PHY controller. It is calculated that total 51% power is saved when HDMI based Video PHY controller is operated 2 GHz for POD_10 instead of LVDCI_15. This power reduction for HDMI based Video PHY controller, when operated at 2 GHz for LVDCI_15 and POD_10 IO Standard is demonstrated in Figure 8.

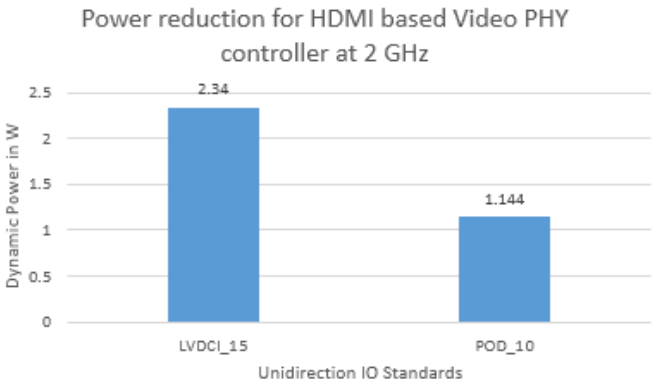

Figure 8. Power reduction of HDMI based Video PHY controller at 2 GHz

Similarly, when, HDMI based Video PHY controller is tested at 6 GHz using LVDCI_15 and POD_10 IO Standard, the dynamic power reduction is achieved. It is showed that for HDMI based Video PHY controller is operated at 6 GHz for LVDCI_15 the total dynamic power was 4.422 W. This dynamic power is compared with design of 6 GHz of for HDMI based Video PHY controller using POD_10 IO Standard that is 1.1669 W. It can be detected that POD_10 IO Standard successfully reduced the power consumption of HDMI based Video PHY controller. It is measure that total 73% power is reduced when HDMI based Video PHY controller is operated 6 GHz for POD_10 as an alternative of LVDCI_15. Figure 9 demonstrates the power reduction for HDMI based Video PHY controller, when operated at 2 GHz for LVDCI_15 and POD_10 IO Standard.

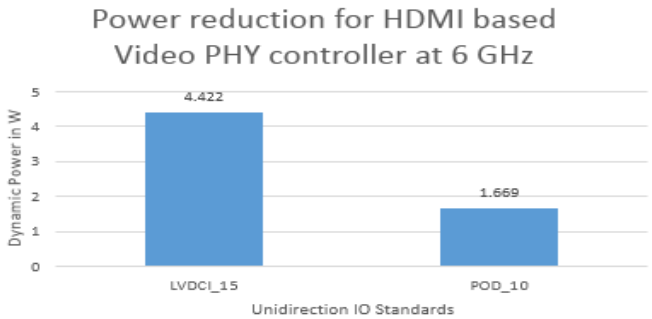

Figure 9. Power reduction of HDMI based Video PHY controller at 6 GHz

Besides the reduction in dynamic power. The reduction in signal power of 30% for POD_10 achieved compared to LVDCI_15 for HDMI based Video PHY controller operated at 2 GHz. The reduction in BRAM power of 53% for POD_10 attained compared to LVDCI_15 for HDMI based Video PHY controller operated at 2 GHz. The reduction in IO power of 70% for POD_10 realized compared to LVDCI_15 for HDMI based Video PHY controller operated at 2 GHz. Similarly, the signal power reduction is signal power of 64% for POD_10 gathered compared to LVDCI_15 for HDMI based Video PHY controller operated at 6 GHz. The reduction in BRAM power of 83% for POD_10 realized compared to LVDCI_15 for HDMI based Video PHY controller operated at 2 GHz. The reduction in IO power of 80% for POD_10 realized compared to LVDCI_15 for HDMI based Video PHY controller operated at 2 GHz. It is determined that POD_10 is reducing power for HDMI based Video PHY controller. The reason for power reduction is that POD IO Standard has low reference voltage and low termination impedance for high performance application. POD IO Standard offers the high performance application for high resolution of HDMI based Video PHY controller. POD offers the DDR4 high speed bus operation for HDMI based

Video PHY controller. This is because the power consumption of POD IO Standard is low compared to LVDCI. Furthermore, the POD IO Standards offer the high performance for HDMI based Video PHY controller.

IV. CONCLUSION AND FUTURE WORK

The low power consumption is achieved for HDMI based Video PHY controller using unidirectional IO Standard for high performance. The HDMI based Video PHY controller is tested for high frequency operation of 2 GHz and 6 GHz using HP IO Standard (LVDCI and POD IO Standards). The dynamic power is calculated for both high frequencies for IO Standards. It is concluded that POD IO Standard offers the low power consumption compared to LVDCI IO Standard. Overall, for 2 GHz design of HDMI based Video PHY controller the 51 % power reduction is achieved and for 6 GHz GHz design of HDMI based Video PHY controller the power reduction of 73% is achieved. The designed GHz HDMI based Video PHY controller will be helpful to produce high resolution video at low power consumption. In the future, the resolution for the HDMI based Video PHY controller can be improved using proposed technique at low power consumption.

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