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# Energy Efficient 10 Gigabit Ethernet Media Access Controller

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*Abstract*—**In this paper, 10 Gigabit Ethernet Media Access Controller (10GEMAC) is designed that consumes less power. The 10 Gigabit Ethernet Media Access Controller is designed by using the different IO Standards available on UltraScale Field Programing Gate Array. The 10G Ethernet Media Access Controller is designed vhdl. The successful design of 10G Ethernet Media Access Controller is operated at high frequencies for different IO Standards. It is defined that the 10G Ethernet Media Access Controller is operated at 10 GHz and 40 GHz. The power consumption is analyzed for the designed 10G Ethernet Media Access Controller, when operated at 10 GHz and 40 GHz. The power consumption is analyzed for Low-Voltage Digitally Controlled Impedance- (LVDCI) IO Standard, and Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) IO Standard. It is determined that when 10G Ethernet Media Access Controller is operated at 10 GHz for LVCMOS IO Standard 20% power consumption is reduced compared to LVDCI IO Standard. When the 10G Ethernet Media Access Controller is operated 40 GHz for LVCMOS IO Standard 52% power reduction is recorded compared to LVDCI IO Standard. The designed energy efficient 10G Ethernet Media Access Controller will be the key component for designing the green network system.**

***Keywords- Ethernet, Media Access Controller, I/O standard, Power analysis.***

## I. INTRODUCTION

An Ethernet Media Access Controller is to integrate the physical Layer devices in the high speed Ethernet networks. The 10Gbps Ethernet (10GE) systems are preferred because in many systems it becomes the standard data rate for high speed communication systems [1-3]. The 10G Ethernet Media Access Controller refers the IEEE 802.3-2012 specification that supports the high-bandwidth for Internet Protocol traffic via LAN, MAN and WAN networks [4]. 10G Ethernet Media Access Controller also provides the interconnection of communications for implementing the emerging interface standards. The 10G Ethernet Media Access Controller an imparted media. It can transmit the heavy data whenever, media access is called. The more data traffic access for 10G Ethernet Media Access Controller will attained more power consumption. In results the devices are overloaded with power consumption, that cause in permanent damage to the 10G Ethernet Media Access Controller. In demonstrating, the low power consumption for different communication devices such as; Pseudo Noise based optical transmitter [5], laser drivers [6] and etc. several low power consumption techniques are utilized. These techniques include; clock gating, voltage scaling [6], variable frequency and etc. every power consumption techniques has its own advantages and disadvantages. It has been significantly discussed by researcher in [7] that power consumption reduction using IO Standard may become the major technique in reducing the power for various devices. In this work, we have designed the 10G Ethernet Media Access Controller via utilizing various IO

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Standard that consumes less power. The 10G Ethernet Media Access Controller is designed to latest Kintex® UltraScale™.

## II. METHODOLOGY

The energy efficient design for the 10G Ethernet Media Access Controller is realized in different steps as defined in Figure 1.

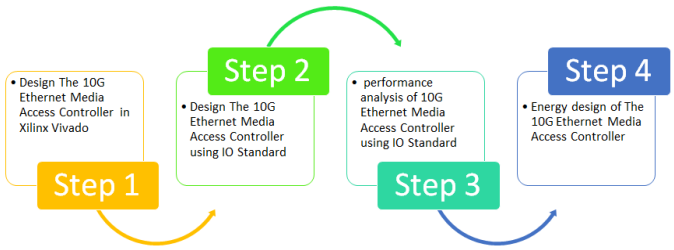


Figure 1. Design steps to developing the energy efficient The 10G Ethernet Media Access Controller

It is defined in Figure 1 that in the first design step, the vhdl based 10G Ethernet Media Access Controller is designed using Xilinx Vivado suite. In the second design step, the vhdl based 10G Ethernet Media Access Controller is designed by programming the vhdl based 10G Ethernet Media Access Controller for different IO Standard. The IO Standard selection is based on the design of the vhdl based 10G Ethernet Media Access Controller. In the third step, IO Standard based 10G Ethernet Media Access Controller performance is demonstrated for different frequencies for different IO Standards using UltraScale Field Programming Gate Array. In the last design step, the IO Standard that consumes least power for the designed 10G Ethernet Media Access Controller is evaluated to be consider for the energy efficient design of 10G Ethernet Media Access Controller.

### *A. Design Step 1: vhdl based 10G Ethernet Media Access Controller*

The 10G Ethernet Media Access Controller is designed in Xilinx Vivado Suite using vhdl. The elaborated/schematic design of 10G Ethernet Media Access Controller is shown in Figure 2.

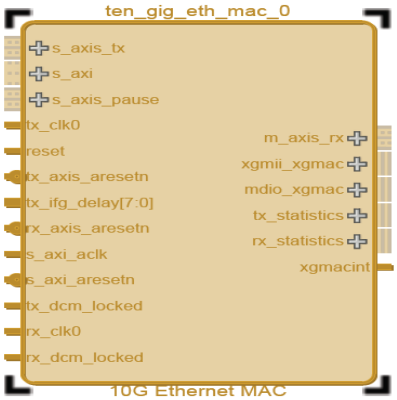


Figure 2. Schematic design of the 10G Ethernet Media Access Controller

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It is demonstrated in Figure 2 that vhdl based 10G Ethernet Media Access Controller is consisted of different pins configuration. The pins that are utilized for the designed 10G Ethernet Media Access Controller are: "s_axis_tx" that is used for serial transmission of bits. "tx_clk0" it is the operating clock frequency of the designed vhdl based 10G Ethernet Media Access Controller. "tx_ifg_delay" it is the delay created by 10G Ethernet Media Access Controller during transmission of bits. "rx_clk0" is the receiving clock in order to synchronize the data transmission between transmitter and receiver.

### *B. Design Step 2: IO Standard based 10G Ethernet Media Access Controller*

In UltraScale FPGA an I/O tile is defined with I/O buffers, I/O logics and I/O delays. Each IOB contains both input and output logic and IO drivers. These drivers can be configured to various I/O standards [8]. The IO Standard based schematic diagram of 10G Ethernet Media Access Controller is demonstrated using Figure 3. It is defined in Figure that 3 device configuration has been changed by adding the IO Standard in VHLD based 10G Ethernet Media Access Controller.

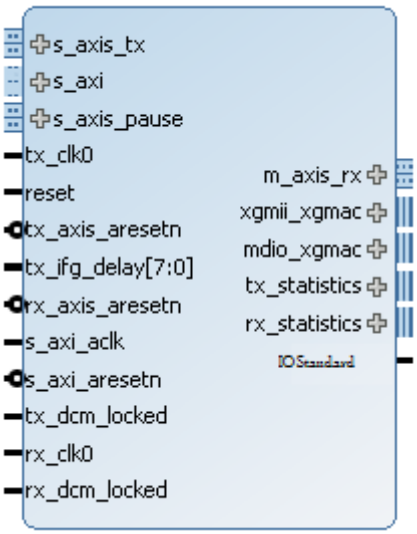


Figure 3. Schematic design of IO based 10G Ethernet Media Access Controller

Virtex UltraScale FPGA support many IO Standard a long list is available in [8]. In this research, authors have selected the specific IO Standards that meet the requirements of communication design. These IO Standards are specified in the Electronic Industry Alliance JEDEC [8]. The IO Standard selected for this research work are as follows:

- LVDCI (Low-Voltage Digitally Controlled Impedance)

  Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

#### *1) LVDCI (Low-Voltage Digitally Controlled Impedance)*

LVDCI IO Standard provides the controlled impedance for I/O buffers. The UltraScale FPGA supports the LVDCI_15, LVDCI_18 defined by (JEDEC). The 10G Ethernet Media Access Controller test bench is verified over LVDCI_18 because this IO Standard support the

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1.8 V for operating the system on FPGA board. The 10G Ethernet Media Access Controller test bench is executed over LVDCI_18. The syntax for changing the IO Standards from default to user defined IO Standards (LVDCI_18) is:

*attribute IOSTANDARD : string;*

*attribute IOSTANDARD of IDIOA0 : label is- "LVDCI_18";*

*2) LVCMOS (Low Voltage CMOS)*

Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) IO Standard is used for high frequency operation. The UltraScale FPGA supports the LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33 defined by (JEDEC). The 10G Ethernet Media Access Controller is tested over LVCMOS18. The syntax for changing the IO Standards from default to user defined IO Standards (LVCMOS 12) is:

*attribute IOSTANDARD : string;*

*attribute IOSTANDARD of IDIOA0 : label is- "LVCMOS18";*

*C. Design Step 3: Performance Analysis of IO Standard based 10G Ethernet Media Access Controller using power analysis*

The performance of IO Standard based 10G Ethernet Media Access Controller is analyzed for high frequency operation of 10 GHz, 40 GHz. The power analysis is performed for these high frequencies using LVDCI, LVCMOS IO Standards for IO Standard based 10G Ethernet Media Access.
The power analysis for 10G Ethernet Media Access in UltraScale FPGA power is comprises of sum of device static power, design static power and design dynamic power presented in equation (1) [8].

$$Total\ FPGA\ power = Design\ Dynamic\ Power + Device\ Static\ Power + Design\ Static\ Power \quad (1)$$

Device static power characterizes the transistor leakage power when devices is powered and not configured. Design Dynamic power epitomizes the power associated with design activity and switching events in the core or I/O of the device. Dynamic power is determined by node capacitance, supply voltage, and switching frequency. Design static power denotes the power consumption when the device is configured with no switching activates. The power consume by clock manager.

*1) Performance Analysis of IO Standard based 10G Ethernet Media Access Controller for 10 GHz frequency via LVDCI IO Standard*

The performance of the 10G Ethernet Media Access Controller is analyzed for 10 GHz for different IO Standards such as; LVDCI and LVCMOS by measuring the on-chip power. The on chip power is measured for dynamic power. Figure 3 defines the on-chip power analysis for 10 GHz at LVDCI IO Standard.

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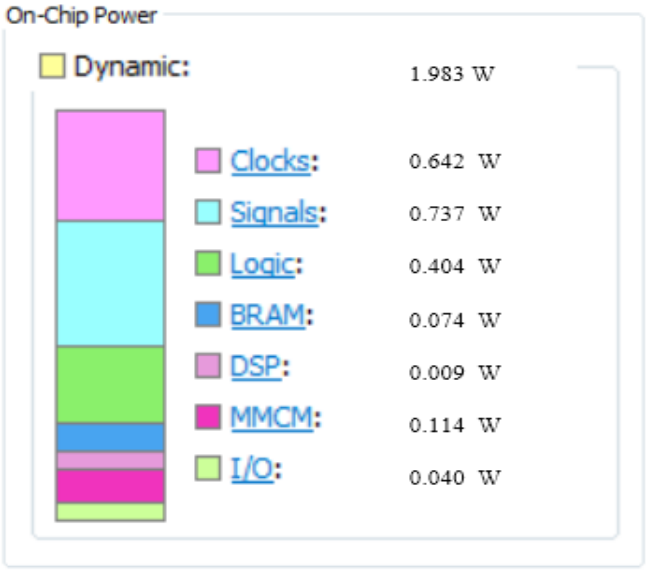


Figure 3. On- Chip Power measurement for 10G Ethernet Media Access Controller at 10GHz for LVDCI IO Standard

It can be analyzed from Figure 3 that 1.983 W dynamic power is consumed by 10G Ethernet Media Access Controller. IO power consumed is 0.04 W.

*2) Performance Analysis of IO Standard based 10G Ethernet Media Access Controller for 10 GHz frequency via LVCMOS IO Standard*

Figure 4 defines the power consumption of 10G Ethernet Media Access Controller at 10 GHz for LVCMOS IO Standard.

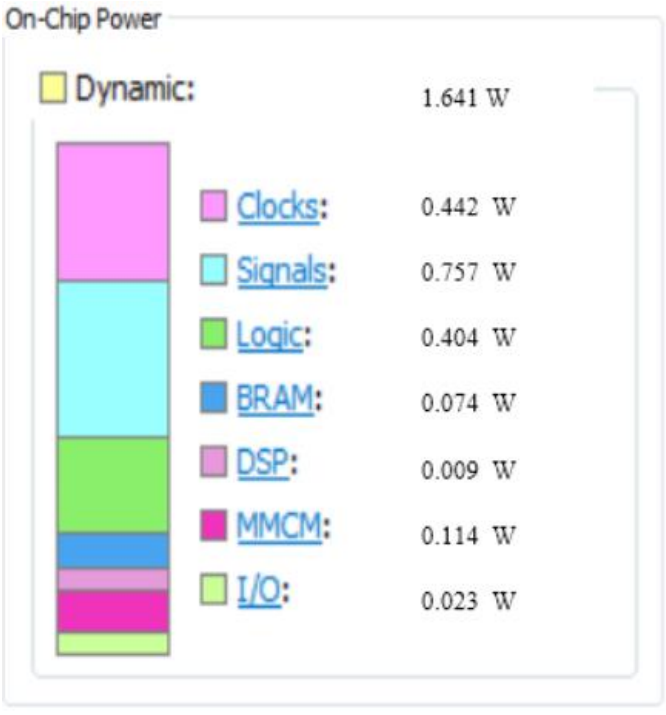

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Figure 4. On- Chip Power measurement for 10G Ethernet Media Access Controller at 10GHz for LVCMOS IO Standard

It can be observed from Figure 4 that dynamic power consumed by 10G Ethernet Media Access Controller is 1.641 W. It can analyzed that IO power is significantly is reduced to 50 %. It is also defined that signal power is also reduced. It is determined that for 10G Ethernet Media Access Controller when operating at 10 GHz for LVDCI and LVCMOS IO Standard. The LVCMOS IO Standard based 10G Ethernet Media Access Controller is consuming less power compared to LVDCI IO Standard. In the next for same IO Standards LVDCI and LVCMOS, 10G Ethernet Media Access Controller is operated on 40 GHz.

*3) Performance Analysis of IO Standard based 10G Ethernet Media Access Controller for 40 GHz frequency via LVDCI IO Standard*

The performance of the 10G Ethernet Media Access Controller is analyzed for 40 GHz for different IO Standards LVDCI and LVCMOS by measuring the on-chip power. Figure 5 defines the on-chip power analysis for 40 GHz at LVDCI IO Standard.

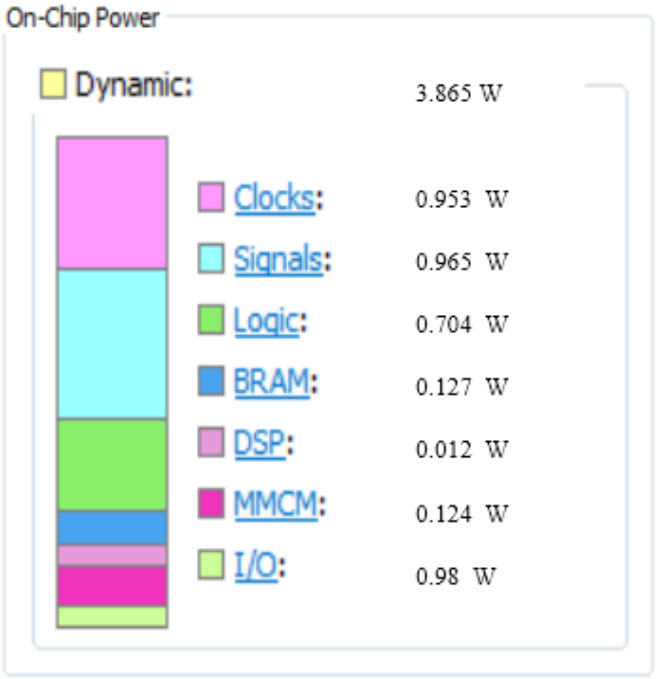


Figure 6. On- Chip Power measurement for 10G Ethernet Media Access Controller at 40GHz for LVDCI IO Standard

It can be observed from Figure 5 that dynamic power consumed by 10G Ethernet Media Access Controller is 3.865 W. The IO Power is 0.98 W for 40 GHz. The signal power is also increased.

*4) Performance Analysis of IO Standard based 10G Ethernet Media Access Controller for 40 GHz frequency via LVCMOS IO Standard*

The dynamic power of 10G Ethernet Media Access Controller for 40 GHz via LVCMOS IO standard is demonstrated in Figure 6. It is defined that total dynamic power consumed by 10G

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Ethernet Media Access Controller is 1.76 W. The IO power consumed is 0.04 W. It can analyzed that IO power is significantly is reduced to LVDCI IO Standard.

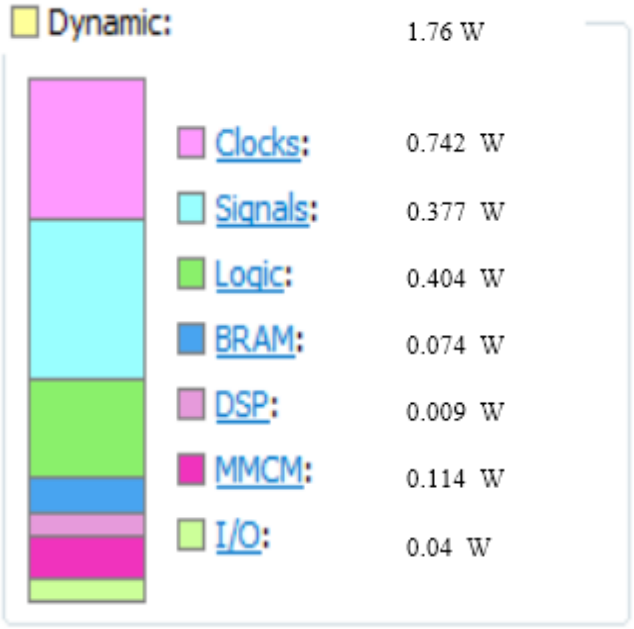


Figure 7. On- Chip Power measurement for 10G Ethernet Media Access Controller at 40GHz for LVCMOS IO Standard

In the next, the attained results are discussed for proposed energy efficient 10G Ethernet Media Access Controller. It is demonstrate that using IO Standards power consumption can be reduced.

## III. Results and Discussion

In this paper, 10G Ethernet Media Access Controller is designed. The designed is realized via UltraScale Field Programming Gate Array. It is demonstrated that IO Standards are significantly reducing the on0cip power consumption for 10G Ethernet Media Access Controller. It is determined that 10G Ethernet Media Access Controller is operated at 10 GHz and 40 GHz frequency. The 10G Ethernet Media Access Controller on-chip power consumption for different frequencies are analyzed by varying the IO Standard. The IO Standard considered for 10G Ethernet Media Access Controller are LVDCI and LVCMOS. It can be observed from Figure 8 that 10G Ethernet Media Access Controllers is operated for 10 GHz via LVDCI and LVCMOS IO Standard the dynamic power reduction is achieved. This power reduction is achieved by decline in IO power.

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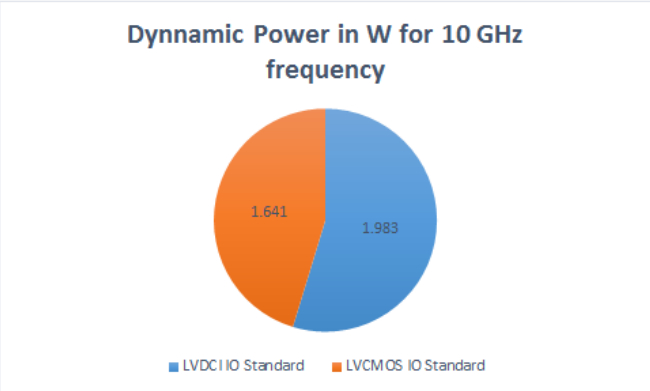


Figure 8. Reduction in Power of 10G Ethernet Media Access Controller at 10 GHz using IO Standard

It is also demonstrated that when 10G Ethernet Media Access Controller is operated at 40 GHz, the dynamic power is reduced significantly. When the 10G Ethernet Media Access Controller is designed using LVDCI IO Standard the dynamic power was 3.865 W, which is very high for practical realization. When, 10G Ethernet Media Access Controller is designed using LVCMOS, the dynamic power is reduced till 1.76 W. The power reduction of 10G Ethernet Media Access Controller for 40 GHz for LVDCI and LVCMOS IO Standard is demonstrated using Figure 9.

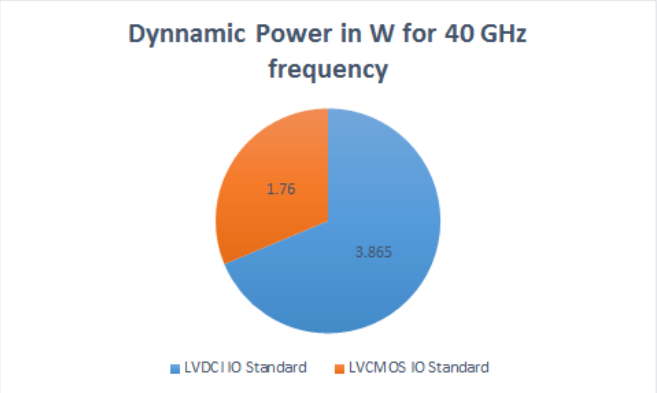


Figure 9. Reduction in Power of 10G Ethernet Media Access Controller at 40 GHz using IO Standard

It is determined that IO Standard are significantly reducing the power for 10G Ethernet Media Access Controller. It is also demonstrate that LVCMOS is producing low power consumption for 10G Ethernet Media Access Controller, when operated at 10 GHz and 40 GHz frequencies. However, for high frequency of 40 GHz, the LVCMOS is pointedly consuming less power. It can be observed that for 10 GHz operating frequency, the dynamic power of 20 % is reduced for 10G Ethernet Media Access Controller. When devices is operated at 40 GHz, the dynamic power of 54 % is reduced for the 10G Ethernet Media Access Controller. The reason behind this less power consumption is that LVDCI IO Standard is operated at core voltage of 1.8 V for 10G Ethernet Media Access Controller. While LVCMOS IO Standard is operated at core voltage of 1.2 V. The change in core voltage is reducing the IO power, which is directly related to dynamic power. It is important to note that this change in core voltage for 10G Ethernet Media Access Controller is practically reliable. The 10G Ethernet Media Access Controller is also tested in real- time via UltraScale Field Programming Gate Array. It is also defined that every device has its own power

consumption behavior for IO Standard. The selection of particular IO Standard for power reduction is also have to be taken care before testing. The irrelevant IO Standard for target device can destroy or damage device permanently.

## IV. CONCLUSION

It is concluded that proposed energy efficient 10G Ethernet Media Access Controller consumes less power for high frequency operation of 40 GHz. The proposed device is designed using IO Standard. The IO Standards are significantly reducing the power consumption of the 10G Ethernet Media Access Controller. The designed energy efficient 10G Ethernet Media Access Controller can be utilized in existing communication networks that will provide the green communication. In future, the energy efficient 10G Ethernet Media Access Controller will be helpful in designing the green communication network.

## V. ACKNOWLEDGEMENT

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